REMARKS

The Official Action dated June 23, 2005 has been received and its contents carefully noted. In view thereof, claims 1, 2 and 4-10 have been canceled in their entirety without prejudice nor disclaimer of the subject matter set forth therein in favor of new claims 11-16 in order to better define that which Applicants' regard as the invention. Accordingly, claims 11-16 are presently pending in the instant application.

With reference now to the Official Action and particularly paragraphs 2 and 4 of the Office Action, claims 1, 4, 6 and 8-10 have been rejected under 35 U.S.C. §102(a) as being anticipated by Japanese Patent Publication No. 03-165058 and claims 2, 5 and 7 have been rejected under 35 U.S.C. §102(e) as being anticipated by or in the alternative under 35 U.S.C. §103(a) as being obvious over the Japanese reference. These rejections are respectfully traversed in that the Japanese Patent Publication neither discloses nor remotely suggests that which is presently set forth by Applicants' claimed invention.

Initially, it is unclear why claims 1, 4, 6 and 8-10 were rejected under 35 U.S.C. §102(a) and claims 2, 5 and 7 have been rejected under 35 U.S.C. §102(e) in that the Japanese Patent Publication applied by the Examiner was published July 17, 1991. However, in view of the following comments, it is respectfully submitted that Applicants' claimed invention clearly distinguishes over the teachings of the Japanese Patent Publication applied by the Examiner.

Again, as noted hereinabove, claims 1, 2 and 4-10 have been canceled in their entirety without prejudice nor disclaimer of the subject matter set forth therein. Accordingly, the following remarks will be directed to new claims 11-16 set forth hereinabove.

That is, new independent claim 11 recites a semiconductor device comprising a plurality of semiconductor elements formed on a substrate, a plurality of through holes which are provided between two adjacent ones of the plurality of semiconductor elements and pass through a surface through a backside of the semiconductor substrate wherein a distance between two adjacent ones of the plurality of through holes is smaller than a thickness of the semiconductor device. Additionally, independent claim 15 recites a semiconductor device comprising a plurality of semiconductor elements formed on a semiconductor substrate, a first group of through holes which are provided between two adjacent ones of the plurality of semiconductor elements and pass through a surface through the backside of the semiconductor substrate and whose side faces are covered with a conductive material and a second group of through holes which are provided in electrodes of the plurality of semiconductor elements, pass through a surface through the backside of the semiconductor substrate, and whose side faces are covered with a conductive material, wherein the conductive material which covers the side faces of the first and second groups of through holes is electrically connected to a wiring layer provided on the backside of the semiconductor substrate and a distance between two adjacent holes of the first group of through holes is smaller than a thickness of the semiconductor substrate. It is respectfully submitted that the Japanese Patent Publication neither discloses nor remotely suggests these features.

As the Examiner can appreciate, each of independent claims 11 and 15 recite a semiconductor device wherein the plurality of through holes are provided between the two adjacent semiconductor elements in the semiconductor substrate and that a distance between the two adjacent through holes is smaller than a thickness of the semiconductor substrate. In

accordance with the present invention it is possible to maintain the strength of the semiconductor substrate while physically suppressing electrical interference between the adjacent semiconductor elements. Particularly, electrical interference between the semiconductor elements which is caused by the semiconductor substrate itself can be reduced.

In order to better understand the teachings of the Japanese Patent Publication, provided herewith is a partial translation of the laid open unexamined Japanese Patent Publication No. 3-165058A. Particularly, the translation is of page 290, the upper left hand column, line 10 to the upper right hand column, line 17.

Therein, it is noted that the semiconductor device disclosed in the Japanese Patent Publication includes an insulator film comprising SiON which is of a thickness of 500 μm over the two semiconductor elements that are provided on the semiconductor substrate; and a plurality of via holes disposed in the orthogonal direction with respect to the substrate between the two semiconductor elements in the insulator film. The distance between the adjacent via holes is 100 μm and the via holes are filled with a metal. This reference further discloses that the via holes, formed to be disposed between the two semiconductor elements in each of the multilayered insulator film and the semiconductor substrate, are connected to each other through a conductor film that is provided between the layers and are grounded at high frequencies. As the Examiner can appreciate from the attached translation an insulating film comprising SiON is formed on the semiconductor substrate, and the via holes are provided in the insulating film in the orthogonal direction to the substrate, thereby separating the two semiconductor elements at high frequency. When the insulating film in which the via holes are formed is thick, it is impossible to form the via holes therein. To address the

problem, the insulating film has a multilayered structure, the via holes are formed in each insulating film and the insulating films are disposed so as not to align the via holes, thereby obtaining the semiconductor device having a stable configuration. The reference further discloses that the via holes provided in the substrate are filled with metal.

That is, the via holes through the semiconductor substrate in each of the insulating films in order to separate the two semiconductor elements by the via holes at high frequency, and the reference stresses that via holes are in the insulating film rather than in the semiconductor substrate.

This is not the case with the present invention. Specifically, the features of the present invention reside in that the plurality of through holes, that is, the first and second groups of through holes, are provided between the two adjacent semiconductor elements on a semiconductor substrate and pass from the surface through the backside of the semiconductor substrate and that the distance between two adjacent holes is smaller than the thickness of the semiconductor substrate. However, as can be appreciated from the attached translation, the via holes of the Japanese Patent Publication are formed only in the insulating film or in the insulating film and the substrate. The via holes are formed in the substrate are not aligned with the via holes formed in the insulating film, and thus the via holes do not pass from the surface through the backside of the semiconductor device. Furthermore, the via holes are filled with conductors such as metal. Consequently, it is respectfully submitted that the Japanese Patent Publication fails to disclose or remotely suggest a plurality of through holes which are provided between the semiconductor elements and pass through the surface and the backside of the semiconductor substrate.

Additionally, in order to suppress the electrical interference between the adjacent semiconductor elements, it is important to form the through holes, that being the first and second groups of through holes in the semiconductor substrate and to control the distance between the through holes, that is, that the distance between the through holes will be smaller than the thickness of the semiconductor substrate. It is noted that the cited Japanese Patent Publication is silent with respect to each of these points.

It has been noted in accordance with Applicants' claimed invention that the reason why it is important to form the through holes in the semiconductor substrate and control the distance between the through holes so as to prevent an electrical interface between the adjacent semiconductor elements is that high frequency is likely to transmit within the semiconductor substrate because the electromagnetic waves have a property of transmitting the medium having a large dielectric constant and the semiconductor substrate has a large dielectric constant. It is known that the semiconductor has a relative dielectric constant larger than an insulator, as noted from "Physics of Semiconductor Devices," second edition, John Willey & Sons, 1981, Appendix H:

Semiconductor	Si:11.9	GaAs:13.1
Insulatoar	SiO_2 : 3.9	Si_3N_4:7.5

Accordingly, even when the insulating film is formed on the semiconductor substrate, high frequency which transmits between the two semiconductor elements, transmits within the semiconductor substrate. Consequently, based on the foregoing, in order to suppress the electric interference between the adjacent semiconductor elements, it has been found that it is important to provide the through holes in a semiconductor substrate and to control the distance between the through holes. It is noted that the Japanese Patent Publication stresses

that the through holes are provided in the insulating film rather than the semiconductor substrate and thus is completely different from that of the present invention. Furthermore, it has been noted by the Applicants that when considering that high frequency transmits within the semiconductor substrate, through holes provided in the semiconductor substrate exhibit a greater effect of separating the semiconductor elements at high frequency than the through holes provided in the insulating film.

Consequently, it is respectfully submitted that Applicants' claimed invention as set forth in each of independent claims 11 and 15 as well as those claims which depend therefrom clearly distinguish over the teachings of Japanese Patent Publication No. 03-165058 and is in proper condition for allowance.

Therefore, in view of the foregoing it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that claims 11-16 be allowed and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,

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